

Abstract of the Disclosure

A test vector decode circuit includes a lockout circuit to prevent inadvertent  
5 latching of output vectors. This circuit is driven by an additional output vector from the  
circuit. The additional output vector, as well as the other output vectors, undergo at least  
one latching. The signal transmitted by the additional output vector as a result of the final  
latching activates the lockout circuit. The test vector decode circuit also receives a  
supervoltage signal. Only by turning off the supervoltage signal can all of the output test  
10 vectors be reset, including the additional output vector.